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PPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,982	11/26/2001	Xia Dai	P9724X	2963
45209 7	590 10/12/2005		EXAMINER	
INTEL/BLAI		YANCHUS III, PAUL B		
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR LOS ANGELES, CA 90025-1030			ART UNIT	PAPER NUMBER
	•		2116	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

h		-				
	Application No.	Applicant(s)				
	09/994,982	DAI, XIA				
Office Action Summary	Examiner	Art Unit .				
	Paul B. Yanchus	2116				
The MAILING DATE of this communication apperent of the second for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period w  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	TE OF THIS COMMUNICATION 6(a). In no event, however, may a reply be tim ill apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONED	L. ely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 19 Ju	ly 2005.					
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This	action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-5 and 10-22</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-5 and 10-22</u> is/are rejected.						
7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or	election requirement					
	o, o out of the transfer of th					
Application Papers						
9) The specification is objected to by the Examiner		Evaminar				
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Ex						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) □ A  □ b) □ Some * c) □ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau	•	d				
* See the attached detailed Office action for a list of the certified copies not received.						
·						
Attachment/s)						
Attachment(s)  1) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)				
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)						
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper Nc(s)/Mail Date	6) Other:	a.c., (ppilodilo)) (1 10-102)				

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## **DETAILED ACTION**

This non-final office action is in response to communications filed on 7/19/05.

## Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-5, 10-12, 15, 16, 18, 19, 21 and 22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 9 of U.S. Patent No. 6,941,480.

Regarding claims 1, 4, 10, 15 and 18 although the conflicting claims are not identical, they are not patentably distinct from each other because as one of ordinary skill in the art would realize, it is well known in the art to supply a clock signal to a processor from a clock generator and it would have been obvious to one of ordinary skill in the art to use a well known clock generator to provide a clock signal to the processor.

Regarding claims 2, 11, 16, 19 and 22, although the conflicting claims are not identical, they are not patentably distinct from each other because as one of ordinary skill in the art would realize, the contents of a processor cache will be maintained when the processor is active.

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Regarding claims 3 and 12, although the conflicting claims are not identical, they are not patentably distinct from each other because as one of ordinary skill in the art would realize, a processor is commonly used to perform graphics controlling operations and it would have been obvious to one of ordinary skill in the art to implement the processor in a graphics device.

Regarding claim 5, although the conflicting claims are not identical, they are not patentably distinct from each other because C0 mode is part of the well known ACPI specification and it would have been obvious to one of ordinary skill in the art to adhere to the well known ACPI specification in order to maximize the system compatibility with other devices and software.

Regarding claim 21, although the conflicting claims are not identical, they are not patentably distinct from each other as one of ordinary skill in the art would realize, switching performance modes of a processor in a portable unit is conventionally done to save power in a portable unit and it would have been obvious to one of ordinary skill in the art to incorporate the teachings of claim 1 of US Patent no. 6,941,480 into a portable unit in order to improve computing performance of the portable unit.

Claims 13, 14, 17 and 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 9 of U.S. Patent No. 6,941,480 in view of Gebara et al., US Patent no. 6,035,407 [Gebara]<sup>1</sup>

Regarding claims 13, 17 and 20, claims 1 and 9 of U.S. Patent No. 6,941,480 does not specifically disclose how the voltage regulator adjusts the voltage supplied to the computer

<sup>&</sup>lt;sup>1</sup> included in previous office action

system component. Gebara discloses a table representation associated with a stepwise ramp that specifies that the voltage level will be adjusted by a predetermined amount of voltage at intervals of a predetermined amount of time [column 8, lines 56-60]. One would be motivated to use the Gebara voltage regulator in the Noble and Clark system to gradually adjust the voltage supplied to the computer system component in order to prevent the voltage regulator overvoltage or undervoltage circuitry from being falsely activated [Gebara, column 8, lines 60-63].

Regarding claim 14, Gebara does not specifically disclose ramping the voltage in 25-50mV steps. However, Gebara does disclose gradually ramping the voltage in steps of a predetermined size and gives an example size of 100mV. It would have been obvious to one of ordinary skill in the art to reduce the voltage step size from 100mV to 25-50mV. One would be motivated enable a more gradual change from the first voltage level to the second voltage level to prevent overvoltage or undervoltage tracking circuitry form being falsely activated [column 8, lines 60-63].

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus October 6, 2005 LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100